WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Friday, May 21, 2004

Hide?	Set Name	Query	Hit Count
		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L47	L44 same reset$4	2
☐	L46	L44 and (power near3 reset$4)	3
☐	L45	L44 same (power near3 reset$4)	0
☐	L44	(control$4 near5 pump) same (monitor$4 near3 power near3 (supply or source))	45
☐	L43	l15 and (monitor$4 near3 power near3 (supply or source))	2
☐	L42	l15 same (monitor$4 near3 power near3 (supply or source))	0
☐	L41	l18 same (monitor$4 near3 power near3 (supply or source))	1
☐	L40	l29 and l18	35
☐	L39	l2 and l18	0
☐	L38	l2 same l15	86
☐	L37	l2 and l15	99
☐	L36	l7 and l11	0
☐	L35	l8 and L29	0
☐	L34	l7 and L29	5
☐	L33	l2 and L29	6
☐	L32	l3 and L29	4
☐	L31	l11 and L29	2
☐	L30	l15 and L29	3
☐	L29	l22 or l23 or l24 or l25 or l26 or l27 or l28	5579
☐	L28	365/189.09.ccls.	1501
☐	L27	365/226.ccls.	1830
☐	L26	323/266.ccls.	245
☐	L25	327/198.ccls.	782
☐	L24	327/143.ccls.	810
☐	L23	713/340.ccls.	435
☐	L22	713/300.ccls.	829
☐	L21	L19.ab.	4
☐	L20	L19.clm.	1
☐	L19	(improv$4 or enhanc$4 or novel) near2 power near2 reset near2 circuit	37

☐	L18	(improv$4 or enhanc$4 or novel) near2 (power near2 reset)	59
☐	L17	L15 and trip$4	14
☐	L16	L15 same trip$4	0
☐	L15	(control$4 near5 switch$4 near5 mode near5 pump$4)	268
☐	L14	L11 and l2	0
☐	L13	L11 and (monitor$4 near3 (power near2 supply$4 or source))	1
☐	L12	L11 and trip$4	6
☐	L11	(power near2 reset) near5 (during near2 start$4)	22
☐	L10	(power near2 reset near5 during start$4)	1731933
☐	L9	(start$4 or post-start$4) same l3	3
☐	L8	(start$4 or post-start$4) same l2	60
☐	L7	(start$4 or post-start$4) and l2	287
☐	L6	L3 and (power near2 reset)	1
☐	L5	L3 and (stability or stable or suitab$7)	8
☐	L4	L3 same (stability or stable or suitab$7)	0
☐	L3	L2 same (power near2 (supply$4 or source))	36
☐	L2	(switch$4 near3 mode near3 pump$4)	569
☐	L1	(switch adj mode adj pump)	0

END OF SEARCH HISTORY

First Hit Fwd Refs

End of Result Set

☐ Generate Collection | Print

L41: Entry 1 of 1 File: USPT Sep 9, 2003

DOCUMENT-IDENTIFIER: US 6618312 B2
TITLE: Method and device for providing a multiple phase power on reset

Detailed Description Text (21):
Therefore, in accordance with various aspects of the present invention, the above method allows reprogramming of the power-on-reset system reset hold times. Thus, in accordance with one aspect of the present invention, a flexibly adaptable power-on-reset device is provided where it is possible to reconfigure the power-on-reset process when a power supply is replaced with a new power supply, or when other modifications are made to the IC device. Furthermore, if, for example, a particular power supply has a quick ramp-up, or if an external power supply monitor is used, the checking process can be disabled entirely. Otherwise the power-on-reset device is programmed to enable the voltage level checking for enhanced reliability. In addition, the ability to reprogram the power-on-reset process enhances the useful life of the integrated circuit by allowing the integrated circuit to be reconfigured and thus modified to meet changing needs.

L47: Entry 2 of 2 File: USPT Aug 16, 1983

DOCUMENT-IDENTIFIER: US 4399200 A
TITLE: Device for controlling a pump in a storage battery

Detailed Description Text (4):
The pump control PC is constructed in accordance with the preferred embodiment of the present invention and is employed with each pump 20, 32 to be controlled. In the illustrated embodiment, two pumps 20, 32, are to be controlled; therefore, two pump control circuits or devices PC are employed. These controls are identical; therefore, only the pump control PC used to control the voltage applied to motor 22 will be described in detail. This description applies equally to the pump control used to apply voltage across motor 34. A single power supply PS is used to control the voltage levels applied to each of the pump controls PC. This power supply forms one aspect of the present invention and is shown in detail in FIGS. 6 and 10D. For the purpose of a general explanation, as shown in FIG. 5, power supply PS includes a command line 120 which receives binary logic from data bus 110, which logic may be latched in an appropriate latch L, such as a flip-flop. As long as a preselected logic is applied to line 120, power supply PS is operated to produce voltage to pump controls PC. The positive output voltage of battery B is applied to power supply PS at line 122. An external 12 volts D.C. is also applied to power supply PS through line 124 connected to the auxiliary lead-acid battery also mounted on vehicle A. The main voltage output of power supply PS is applied to line 130. This voltage output varies in accordance with the graph shown in FIG. 7A and is ultimately the voltage level of battery B. Power supply PS also creates an internal 12 volts voltage in line 132. Thus, the output of power supply PS is essentially an internal 12 volts supply (12 V INT), on line 132 and a main voltage on line 130. Both of these voltage levels are directed to the input of pump control PC. As is apparent from FIG. 10D, power supply PS monitors the voltage of battery B and produces a monitoring signal in lines 174. These lines are directed to data bus 110 for use by microprocessor 100. In practice, if the voltage of battery B exceeds approximately 74 volts D.C., latch L is reset and the command logic in line 120 is removed to transfer control of the input voltage to pump controls PC from the auxiliary or external voltage supply of line 124 through the main power bus of battery B attached to line 122.

L46: Entry 1 of 3 File: USPT Apr 27, 2004

DOCUMENT-IDENTIFIER: US 6727681 B2
TITLE: Power supply circuit and control method for the same

Detailed Description Text (145):
After activating a reset when the system power turns on, the host activates the LCD controller 60 (CPU1). This can be achieved by, for example, canceling the LCD controller 60 reset.

Detailed Description Text (163):
The power supply circuit then monitors the step-down potential or output potential (PWB3). When the power supply circuit rise stabilizes as determined by the monitored results, the power supply circuit controls switching from the potential of the potential-adjusted power supply potential VDD to the potential of the potential-adjusted step-down potential VREF1 (PWB4), and thereafter supplies the potential generated by the charge pump step-down circuit to the LCD controller (PWB5).

First Hit Fwd Refs

End of Result Set

Generate Collection Print

L32: Entry 4 of 4 File: USPT Jun 30, 1998

DOCUMENT-IDENTIFIER: US 5774405 A
TITLE: Dynamic random access memory having an internal circuit using a boosted potential

Detailed Description Text (89):
Power supply potential detecting circuit 151 may have the same structure as that in FIG. 17 or 18. When it is determined by the power supply potential detecting circuit 151 that the level of power supply potential Vcc is lower than a predetermined level, switch signal SS at "L" level is issued to charge pump circuit P7. Thereby, charge pump circuit P7 can issue boosted potential Vpp2 of 3Vcc at the maximum in accordance with switch signal SS at "L" level. When it is determined by power supply potential detecting circuit 151 that the level of power supply potential Vcc is higher than the predetermined level, switch signal SS at "H" level is issued to charge pump circuit P7. Thereby, charge pump circuit P7 can issue boosted potential Vpp2 at 2Vcc level at the maximum in accordance with switch signal SS at "H" level. The capability of charge pump circuit P7 is thus switched irrespectively of the operation mode. Charge pump circuit P7 issues boosted potential Vpp2 to word driver 63 in response to clock signal CLK sent from ring oscillator 55. Detecting circuit D2 detects the potential level of boosted potential Vpp2, and controls the operation of ring oscillator 55 to maintain boosted potential Vpp2 at the second level required by word driver 63.

Current US Original Classification (1):
365/226

L30: Entry 2 of 3 File: USPT Jun 27, 2000

DOCUMENT-IDENTIFIER: US 6081472 A
TITLE: Cell refresh circuit of memory device

Current US Cross Reference Classification (1):
365/226

CLAIMS:

15. The circuit of claim 12, wherein the power input circuit comprises:

a power selecting controller that outputs one of a program mode signal and a write signal as a power selecting control signal;

a power supply unit that outputs the program voltage, the source voltage and the pumping voltage as an output voltage; and

a power switching unit that selects the output voltage from the power supply based on the power selecting control signal, and wherein the power supply unit comprises,

a charge pumping circuit that generates the pumping voltage by pumping the source voltage, and

a selecting circuit that selects the program voltage in the program mode and an output voltage from the charge pumping circuit in the operation mode to output to the power switching unit, and wherein the power selecting controller and the selecting circuit comprise a logic-gate.

19. The circuit of claim 18, wherein the power supply unit comprises a selecting circuit that selects the program voltage in the program mode and an output voltage from the pumping circuit in the operation mode to output to the power switching unit, and wherein the power selecting controller and the selecting circuit comprise a logic-gate.

First Hit Fwd Refs

End of Result Set

Generate Collection Print

L30: Entry 3 of 3 File: USPT Mar 30, 1999

DOCUMENT-IDENTIFIER: US 5889723 A
TITLE: Standby voltage boosting stage and method for a memory device

Detailed Description Text (28):
Advantages of the circuit described above include the following. By monitoring the operating condition of the pump prior to switching to standby, this embodiment appropriately controls operation of the pump in standby mode, and more specifically provides for automatically 25 enabling and disabling the pump according to the voltage supply used in the device during active operation. Standby operation of the pump may be performed at different frequencies, depending on the settings of nonvolatile (but programmable) memory elements 11a, 11b, e.g., to take into account the operating temperature of the device, which determines losses at various levels; active operation of the pump may be selectively free-running or regulated.

Current US Cross Reference Classification (1):
365/226

First Hit Fwd Refs

End of Result Set

Generate Collection | Print

L31: Entry 2 of 2 File: USPT Nov 13, 1990

DOCUMENT-IDENTIFIER: US 4970408 A
TITLE: CMOS power-on reset circuit

Brief Summary Text (2):
The present invention relates in general to power-on reset circuits, and more particularly, to a CMOS power-on reset circuit for providing an output signal during system start-up as the power supply voltage reaches a predetermined magnitude.

Current US Original Classification (1):
327/143

L34: Entry 1 of 5 File: USPT Oct 29, 2002

DOCUMENT-IDENTIFIER: US 6473321 B2
TITLE: Semiconductor integrated circuit and nonvolatile semiconductor memory

Brief Summary Text (26):
The configuration described above permits control to reduce power consumption by stopping the operation of one of the charge pumps according to the mode of operation or by switching the frequency of operating clocks, and to reliably generate a boosted voltage of a desired level even if the source voltage is low.

Detailed Description Text (7):
The clocks CK1, CK2, CLK1, CLK2 and PCLK2 are supplied from a clock generator (see reference numeral 34 in FIG. 9) within the chip. The configuration is such that the supply of the clocks to the charge pumps CP11, CP21 and CP22 can be intercepted by gates 7a, 7b and 7c controlled by start signals ST1, ST2 and ST3 from a control circuit, and any charge pump to which clock supply is intercepted stops boosting the voltage.

Detailed Description Text (10):
More specifically, in the flash memory according to this embodiment, while the charge pump CP12 for generating the boosted voltage VCP operates in any mode of operation, i.e. all the time, because it supplies operating power to the internal logic gate circuit 4 and the resistance dividing circuit 6 which constitute resistive loads, the operation of the charge pump CP11 to generate the boosted voltage VWDP is stopped to save power consumption in the reading mode, wherein no high boosted voltage is required. When the operation of the charge pump CP11 to generate the boosted voltage VWDP is stopped, the operations of the charge pumps CP21 and CP22 of the voltage booster circuit 2 for carrying out the second stage of voltage boosting on the basis of this boosted voltage VWDP are also stopped. The operations of the charge pumps CP11, CP21 and CP22 can be stopped by suspending the supply of operating clocks with the start signals ST1, ST2 and ST3.

Detailed Description Text (60):
The MOSFET Qc1 in the resistance dividing circuit 531 is a switch to make it possible to let a current flow to the resistors R1 and R2 or to intercept the flow under control with a start signal ST so as to activate this switching control circuit 53 only when the charge pump CP20 for the second stage of voltage boosting is operating (when writing into or erasing any content from the flash memory). Incidentally, as this start signal ST, a signal of the logical sum of the control signals ST2 and ST3 in the embodiment shown in FIG. 1 can be used. The application of this arrangement results in the failure of the output of the charge pump CP20 for the second stage of voltage boosting, which reached the target voltage where the external source voltage Vcc was 3 V-based even if the clock frequency was high as shown in FIG. 12(a), to reach the target voltage where the external source voltage Vcc is 1.8 V-based if the clock frequency is high as shown in FIG. 12(b). However, by lowering the clock frequency as shown in FIG. 12(c), the output of the charge pump CP20 for the second stage of voltage boosting can eventually attain the target voltage even though it takes a longer time.

Detailed Description Text (62):
In the embodiment shown in FIG. 13, there is provided an AND gate 61 the control

signal for which is the output signal LMD of this limiter circuit 60. The start signal ST for the charge pump CP20 is controlled with the limiter output LMD, and when the output boosted voltage of the charge pump CP20 has surpassed a desired level, the operation of the charge pump CP20 can be stopped to reduce wasteful power consumption.

Detailed Description Text (63):
Further, the flash memory shown in FIG. 9 can be so configured as to supply the limiter output LMD to the control circuit 32 to let the control circuit 32, in response to the variation of this limiter output LMD to a high level, start applying a write or erase voltage to the memory cells. This makes possible combined use of the circuit shown in FIG. 13 and that shown in FIG. 11 to provide the flash memory with the combination so that, no matter whether the external source voltage Vcc of the system is 3 V-based or 1.8 V-based, accurate writing and erasion can be executed in exactly the same sequence even though the length of time required differs, resulting in expanded versatility of the chip.

Current US Cross Reference Classification (2):
365/226

L31: Entry 1 of 2 File: USPT Sep 12, 1995

DOCUMENT-IDENTIFIER: US 5450417 A
TITLE: Circuit for testing power-on-reset circuitry

Brief Summary Text (6):
The problem is to find an efficient way to determine, without probes or dismantling, whether or not the power-on-reset circuitry of an integrated circuit generates a power-on-reset pulse during the start-up (power-up) sequence of operation.

Current US Cross Reference Classification (1):
327/198

L12: Entry 3 of 6 File: USPT Feb 19, 1985

DOCUMENT-IDENTIFIER: US 4500821 A
TITLE: Speed or torque control circuit for an electronically commutated motor (ECM) and method of controlling the torque or speed of an ECM

Detailed Description Text (57):
During start conditions the Autonull sequence is affected by the Power On Reset 150. The Power On sequence is illustrated in the waveforms of FIG. 12B. When power is first applied, the POR waveform is in an active low which causes the Null Clock waveform (D17 Q) to go high. This causes the Autonull counter to be preset in a high offset current condition. When the POR waveform goes to an inactive high subsequently, the Null Clock waveform falls, allowing the counter in the Autonull Circuit to decrement. The autonulling is further affected by the application of an offset current IST which is interrupted during nulling, but active during capacitor resetting and integration. The offset current IST adds to the discharge current of the Integrating Amplifier and causes the integrating capacitor to discharge more rapidly and more positively toward the threshold of comparator COM 2. Under the influence of the logic contained in the POR block, the IST current continues until 5 autonull sequences are completed. During the same 5 count sequence, the lower drivers BOBA-C are also disabled so that no power is applied to the motor windings. On the sixth count, the IST and I Start highs are terminated, the motor windings are energized and autonulling continues in the normal manner.

Detailed Description Text (111):
The operation of the wall control 105 involves the components earlier named connected to the Regulate pad P14. These include the transistor Q81 and resistors R25, R26, R27, R29, R30 and R40. Operation of the wall control adjusts the average voltage applied to the motor. The maximum voltage (e.g. 135 volts) produces the maximum speed. Decreasing the average voltage by means of the wall control produces a substantially linear reduction in voltage applied to the motor as indicated by the upper solid line. (When this reduction begins, let us assume that R40 is set at the maximum value.) At the maximum value, Q81 is biased off by an approximately 1.4 volts difference between its emitter voltage, which is defined by the Zener diode CR1 at 9 volts above ground, and the base voltage, which is defined at about 10.4 volts by the voltage divider formed by R26 and R27 connected between the 135 V B+ terminal and ground. As the B+ potential is adjusted down, the voltage on the emitter connected to the Zener diode remains constant, while the voltage on the base connected to the voltage divider falls in proportion to the reduction in B+ potential. At point 110 V B+, the reverse bias on Q81 is removed, and adequate forward bias provided to overcome the junction drop, and initiate conduction. To this point, in the downward adjustment of the potential, the voltage on the Regulate pad P14 has been unaffected, and has remained at zero potential. Beyond this point, conduction by transistor Q81 between Vdd and the Regulate pad causes the voltage on the pad to increase. Any slight increase in voltage raises the threshold of U89, and causes a decrease in the Pulse Width. The joint reduction in absolute B+ voltage and in the duty cycle produces an increased rate of decrease in average voltage. At about 60 volts, a minimum rotation rate (just above the stalling speed of the motor) is achieved and the PWM duty cycle is near zero. For a REG voltage equal to about 2.2 volts, the PWM duty cycle and speed are both zero. At this point any further decrease in voltage provides no further decrease in speed of the motor, but rather a further elevation of the voltage on the Regulate pad.

This last range of adjustment permits the voltage increase on the Regulate pad to signal a reversal in rotation by tripping a comparator set at 2.4 volts, as will be described in connection with the Forward/Reverse Logic 149.

First Hit Fwd Refs

End of Result Set

Generate Collection Print

L20: Entry 1 of 1 File: USPT Mar 16, 1982

DOCUMENT-IDENTIFIER: US 4320386 A
TITLE: Selection and power reset circuit

CLAIMS:

1. An improved selection and power reset circuit for use with a plurality of programming devices each having a respective power input which, when energized, energizes its respective programming device, and for use with a computer device coupled to said programming devices and having a reset input, said selection and power reset circuit comprising:

a. a programming switch having a power input terminal, and having a plurality of power output terminals for respective connection to said power input terminals of said programming devices, said programming switch selectively connecting its power input terminal to one of its power output terminals;

b. a time delay capacitor for connection to said power reset input of said computer device;

c. a charge-discharge circuit having first and second terminals, said second terminal being connected to said time delay capacitor, said charge-discharge circuit providing a relatively high impedance to current flowing between said first and second terminals in a first direction and a relatively low impedance to current flowing between said second and first terminals in a second opposite direction;

d. and a device respectively connected between each of said power output terminals of said programming switch and said first terminal of said charge-discharge circuit to provide a relatively low impedance to current flowing in said first direction between said output terminals of said programming switch and said first terminal of said charge-discharge circuit;

e. whereby said time delay capacitor receives a first charge condition in response to power at one of said power output terminals of said programming switch, and receives a second charge condition in response to the relatively short absence of power at all of said power output terminals of said programming switch.

2. The improved power reset circuit of claim 1 wherein each of said devices comprises a diode rectifier poled to provide said relatively low impedance to current flowing in said first direction.

3. The improved power reset circuit of claim 1 or claim 2 wherein said charge-discharge circuit comprises a diode rectifier and resistor connected in parallel between said first terminal and said second terminal, said diode rectifier poled to provide said relatively high impedance to current flowing between said first and second terminals in said first direction, and to provide said relatively low impedance to current flowing between said first and second terminals in said second opposite direction.

First Hit

End of Result Set

Generate Collection Print

L9: Entry 3 of 3 File: DWPI Jul 30, 1976

DERWENT-ACC-NO: 1977-C0416Y
DERWENT-WEEK: 197710

TITLE: Marine electric pump remote control unit - has self interlock relay, preventing auxiliary pump self start up

Basic Abstract Text (2):
Either of the pumps can acct as the main or auxiliary one - the selection is made by a switch. The unit operates in the following way. The main pump is started by a mode switch and if there is pressure in the delivery line, the pressure sensor contact causes a relay to self-interlock, preparing the auxiliary pump starting relay power supply, via the other pressure sensor contact. If suction pressure drops, this contact supplies the auxiliary pump starting relay, which interlocks, and its contact prepares the stopping relay supply line via the pressure sensor contact. The auxiliary pump starts up, and when delivery pressure has been restored, the pressure sensor contact energises the pump stopping relay, whose contacts cut off the supply of only the main pump's contactor.

L5: Entry 6 of 8 File: USPT Oct 8, 1991

DOCUMENT-IDENTIFIER: US 5055840 A
** See image for Certificate of Correction **
TITLE: Infrared touch input device and light emitted activation circuit

Brief Summary Text (8):
It is another object of this invention to provide a generally stable current so that the current though each LED is normalized to reduce variations in current through the various LEDs in the individually addressable matrix. Therefore the light levels around the LED matrix tend to be more constant.

Detailed Description Text (4):
FIG. 2 shows arrays of light emitting devices and arrays of light detecting devices disposed around the periphery of an irradiated field 12. A touch input device, as depicted herein, when used with the display of a CRT, would be configured in this manner, with two orthogonal arrays of light emitting devices and two orthogonal arrays of photodetectors disposed along the sides of a rectangular display area 12. Light emitting diodes and phototransistors are commonly used for such touch input systems, although it should be understood that other light emitting devices and light detecting devices could be suitably employed. As shown herein, a Y array of light emitting diodes (LEDs), Y1 through YN, are located along the left of the 20 surrounding the display area or irradiated field 12. A similar array of light emitting diodes, X1 through XN, is located along the bottom of the frame 20. Arrays of phototransistors, X'1 through X'N, located along the top of the frame 20 and Y'1 through Y'N located along the right side of frame 20 are disposed such that individual corresponding LED's and phototransistors, such as X1-X'1 and X2-X'2 and Y1-Y'1 and Y2-Y'2, are aligned. Thus, when light is emitted by an individual light emitting device, such as X1, this light will be incident upon a corresponding aligned phototransistor X'1. FIG. 2 shows, however, that the light emitted by individual LEDs or other light emitting devices is incident not only upon the corresponding aligned photodetector but is also incident upon adjacent photodetectors. Note that while the light emitted along centerline 22 between emitter-detector pairs X1-X'1 will be incident on detector X'1, light emitted along line 24, within the dispersion angle of conventional light emitting devices, will be incident upon adjacent phototransistor X'2. Light indicated at 26 and 28 might also be incident upon sides of the frame 20 causing certain glare and reflection problems in practical touch input systems. A common method of ensuring that light emitted by a given light emitting device, X1, detected only by the corresponding light detecting device or phototransistor, X'1, and not by an adjacent light detecting device such as X'2, is to sequentially activate light emitting devices and sequentially scan the arrays of phototransistors. In other words, when a given light emitting device is activated and emits light, only the aligned phototransistor, is activated although the adjacent phototransistors are illuminated. Thus, activation of light emitting diode X1 would occur at the same time that phototransistor X'1 is activated to detect incident light. The adjacent phototransistor X'2, upon which light from LED X1 would also be incident, would not be turned on during the interval in which LED X1 is activated. Note that this sequential and synchronized activation of light emitting diodes and phototransistors permits accurate detection of the presence of an opaque element positioned between aligned LEDs and phototransistors. The light from an adjacent LED, which is not blocked by an opaque element disposed in the field, will not

activate a "blocked" phototransistor simply because that LED will not be turned on during the activation interval of the "blocked" phototransistor. This sequential activation of light emitting devices and light detecting devices is achieved by conventional multiplexing techniques with scan rates of about twenty scans per second.

CLAIMS:

21. A touch input device for detecting the presence of an opaque element, comprising:

a plurality of sequentially activatable light emitting elements individually aligned with a plurality of light detecting elements, light from each one of said light emitting elements being incident upon an associated one of said light detecting elements unless interrupted by the presence of an opaque object;

means for activating said light emitting elements including:

a common voltage source generating a supply voltage;

a common charge pump means switchable between a charge mode and an activating mode, said charge pump means being electrically connected in series with said voltage source to a respective one of said light emitting elements upon activation thereof by said activation means to transmit power to said one of said light emitting elements from both said voltage source and said charge pump means simultaneously, said charge pump means adapted to store a voltage of up to an amount approximately equal to said supply voltage during said charge mode, and during said activating mode to supply power to a said respective one of said light emitting elements at a voltage greater than said supply voltage; and

control means for generating a first signal and a second signal, said fist signal selecting an individual one of said light emitting elements, each said individual one of said selected light emitting elements being activated by changes in said second signal and said charge pump means being switched from the charge mode to the activating mode by changes in said second signal and thereby being synchronous therewith,

whereby the common charge pump means and common voltage source insure that the light emitted by each said light emitting element exceeds a minimum threshold, while synchronous operation of said charge pump means results in generating minimal electrical noise and thereby maintaining the integrity of the functioning of the touch input device.

L21: Entry 1 of 4 File: USPT Mar 20, 2001

DOCUMENT-IDENTIFIER: US 6204703 B1
TITLE: Power on reset circuit with power noise immunity

Abstract Text (1):
A power on reset includes a latch controller and a latch circuit. The latch controller sets the latch circuit to an initialization state when a power supply voltage is less than a first threshold voltage during power-up, so that a power on reset signal from the latch circuit has the power supply voltage, a logical high level (i.e., goes to a logically activated state). The latch controller resets the latch circuit when the power supply voltage becomes higher than a second threshold voltage which is higher than the first threshold voltage, so that the power on reset signal goes to the ground voltage Vss, a logical low level (i.e., goes to a logically inactivated state). According to such a circuit configuration, even though the power supply voltage oscillates around a voltage at a point in time when the power on reset signal transitions from the power supply voltage to the ground voltage, the power on reset signal continues to be maintained at a previous set state. This prevents logic elements, to be set at a desired state during power-up, from performing needless operations because of the power oscillation. Therefore, the power on reset circuit according to the present invention has an improved power noise immunity.

L21: Entry 2 of 4 File: USPT Sep 3, 1996

DOCUMENT-IDENTIFIER: US 5552725 A
** See image for Certificate of Correction **
TITLE: Low power, slew rate insensitive power-on reset circuit

Abstract Text (1):
An improved power-on reset circuit is provided for controlling reset signal transition until after the power supply has achieved operational levels. Specifically, the reset signal is designated to transition from a high to a low state after the power supply exceeds a fixed reference voltage. The reference voltage is set at a voltage value greater than the operational voltage level of devices within a load circuit connected to the output of the power-on reset circuit. The power-on reset circuit includes numerous subcircuits used to define the reference voltage, trigger the reference voltage in relation to the power supply voltage, delay the triggered voltage, and buffer the delayed, triggered voltage to a reset value capable of driving load circuit impedances.

L5: Entry 1 of 8 File: USPT Apr 9, 2002

DOCUMENT-IDENTIFIER: US 6369552 B2
TITLE: Regulated auxiliary power supply

Detailed Description Text (9):
The circuit of FIG. 1, however, still suffers from the problem of operation in the reconfiguration mode since although the microcontroller 32 now has a stable power supply when the SMPS is off, is it desirable to reduce the overall cost of the SMPS power supply.

CLAIMS:

9. In a switched mode power supply having an integrated circuit controller to provide voltage regulation, and having a source of varying voltage, the switched mode power supply being operable in a normal mode and in a standby mode in which the output voltage is substantially reduced, a circuit for powering the controller during standby mode comprising:

a charge pump circuit having an input and an output, the input coupled to the source of varying voltage for receiving power therefrom, the output coupled to the input power supply terminal of the integrated circuit controller, and a switch coupled to the charge pump for controlling the voltage output of the charge pump when the switched mode power supply is in standby mode.

L5: Entry 4 of 8 File: USPT Dec 14, 1999

DOCUMENT-IDENTIFIER: US 6002630 A
TITLE: On chip voltage generation for low power integrated circuits

Detailed Description Text (12):
FIG. 3 provides a simplified diagram of the supply voltage sensor 32 of FIG. 1. The supply voltage is applied at node 100 in FIG. 3. A first resistor R1 and a second resistor R2 are coupled in series between node 100 and ground. Node 101 is found between resistors R1 and R2. Node 101 is connected to the first input of a comparator 103 and a reference potential is supplied on a second input 104 to the comparator 103. The output of the comparator is the signal VHH which is applied on line 80 in FIG. 2. The comparator is used to detect the voltage level of the external power supply VDD. The comparator relies on a stable Vref on line 104. A preferred reference voltage is approximately 2 volts given a power supply of 2.7 volts to 3.6 volts. By appropriately selecting the ratio the resistors R1 and R2, the trip point of the comparator can be set. For example, if R1:R2=3:5, then the trip voltage is equal to 3.2 volts. In this case, the output VHH will be a logic 1 if the supply potential is greater than or equal to 3.2 volts, and a logic 0 otherwise.

Detailed Description Text (23):
FIG. 5 is a circuit diagram of the comparator 103 shown in FIG. 3 for one example implementation. According to the example illustrated where VDD is specified for the range between 2.7 and 3.6 volts, the resistors R1 and R2 of FIG. 3 are implemented by resistor 300 and resistor 301. The inputs to the comparator include the reference voltage VREF at node 302, and the divided supply potential at node 304. The supply potential is divided down by resistors 300 and 301. The reference voltage at node 302 is set to about 2 volts using a stable reference supply. The trip point of the comparator of FIG. 5 is determined by the selection of the values of the resistors 300 and 301. For example, if the ratio of resistor 300 to resistor 301 is about 3 to 5, then the trip point is about 3.2 volts. This results in the output VHH at node 305 being high if the supply potential at node 303 is above 3.2 volts, and low if the supply potential is below 3.2 volts.

Detailed Description Text (37):
The design parameters of the auxiliary pump are dependent on the boosted level that can be reached by the boost circuit. If the boost circuit alone is able to pull the AVXS node to a voltage level high enough for the read mode, no auxiliary pump is necessary. However, if the boost circuit alone is not enough to reach the desired range, then an auxiliary pump must be used. For example, if the target read mode AVXS range is 4.5 to 5.2 volts, and the power supply voltage is about 2.7 volts, the boost circuit is able to boost the node AVXS to about 4.2 volts. In this case we need the auxiliary pump to supplement the boost circuit so as to pull the final level of AVXS to above 4.5 volts, for example 4.6 volts. The auxiliary pump is able to supply the 0.4 voltage difference in this case. Furthermore, if after each word line switch, the AVXS drops to 3.2 volts, the read pump must be designed to supply at least 1.3 volts of difference. Thus, the read pump cannot be utilized as the auxiliary boost pump, because it would result in charging the AVXS level to a level which is too high as can be determined by adding the 1.3 volt read pump boost to the 4.2 volt boost circuit result. This shows a 5.5 volt value which exceeds the target range of 4.5 to 5.2 volts. In this case, an auxiliary pump is necessary. In

another scenario, if the AVXS node drops to 4 volts after each word line switch, the read mode pump needs to be designed to pull the node from 4 volts back to about 4.5 volts. This is only a 0.5 volt difference. Consequently, the read pump can be utilized as the auxiliary pump, and still fall within the design target.